

In re Patent Application of:

KLIESNER ET AL.

Serial No. 10/620,151

Filed: 07/15/2003

REMARKS

Claims 1-15 remain in the application. Claims 1-15 stand rejected. No claims have been amended.

In the final rejection, the Examiner withdrew the previous rejection in light of Applicants' response. However, the Examiner entered a new ground of rejection of all of the claims.

The Examiner rejected claims 1-15 under 35 U.S.C. § 103 as unpatentable over Vergnes et al. in view of Perrott.

In response to the new grounds of rejection in the final rejection, Applicants filed a Request for Reconsideration under 37 C.F.R. § 1.116. In response to the Request for Reconsideration, the Examiner entered an Advisory Action dated December 3, 2007, which indicated the application was not in condition for allowance.

Concurrently herewith, Applicants have filed a Request For Continued Examination. In conjunction with that Request For Continued Examination, Applicants respectfully request that the Examiner reconsider the rejection in view of the following comments.

Each of the independent claims in this application is directed to a clock recovery circuit which derives "an output clock signal from a received data signal."

The Vergnes et al. reference is not directed to a clock recovery circuit. Rather, it is directed to a frequency synthesizer.

Each of the independent claims of this application requires a series connection of "an error filter, a gain element and a

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frequency accumulator." Vergnes et al. does not teach or suggest the use of a gain element.

The purpose of the claimed gain element in that series connection is set forth on page 7 of the specification, lines 4-12. There, the Applicants state:

The output of the phase detector/comparator 50, which represents the error between the recovered clock and the received data signal, is coupled through a loop filter 60 and gain stage 70 for application to a frequency accumulator 80. The gain is set so that the accumulator 80 overflows when the difference frequency f_d between the received data clock f_R and frequency f_N is a prescribed value.

Thus, the gain stage provides for control of overflow/underflow.

In the advisory action of December 3, 2007, the Examiner makes two assertions:

As well known in the art that [sic] the second order phase locked loop inherently includes closed loop gain. (page 2 of the advisory action, paragraph 2)

The use of a loop amplifier is to increase the loop again of the phase locked loop as common knowledge of one of ordinary skill in the art. (page 2 of the advisory action, paragraph 3)

Applicants challenge the Examiner's taking of official notice in these two quotations and request that the Examiner provide proof of the matters for which the Examiner takes official notice.

With respect to the first assertion of official notice, the Examiner asserts that the "second order phase locked loop

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inherently includes closed loop gain." However, the Examiner has not shown that Vergnes et al. is a second order phase locked loop and that it inherently includes closed loop gain. The Examiner's statement on its face does not specify the amount of gain whether it is positive, negative or fractional in nature. In certain general phase locked loops, positive gain would result in oscillation and not stability. The Examiner has not shown that the application of gain in the Vergnes et al. reference would result in an operative system. The same question applies to the second assertion of official notice. A positive gain, in excess of unity, may well result in instability. In both instances, the Examiner has failed to explain why, even if his assertions were true, it would be obvious to include those in Vergnes et al. The only motivation for such an inclusion would be to meet the terms of the claim language.

Figure 1 of Vergnes et al. is directed to a frequency synthesizer. Figures 6 and 7 of Vergnes et al. refer to phase lock loops using the synthesizer of Figure 1 in two different embodiments (Figure 6 and Figure 7). The Examiner has relied upon the embodiment of Figure 6 for the rejection.

All embodiments shown in Vergnes et al. have an output frequency that is determined by digital words. Turning to column 6, lines 53-60 state:

The phase signal is generated on the transmitter side by means of a phase generator (a modulo counter). This counter is periodically transmitted in a bitstream time clock and this value, a digital tuning word, represents the digital value of the phase. On the receiver side, this digital value must be recovered and filtered, in order to cope with channel disturbances. The recovered, compared and filtered signal will drive a frequency synthesizer.

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Considering Figures 1, 6 and 7 of Vergnes et al., the input tuning words which arrives at the integrators in the respective Figures, are digital words. Digital words are integrated by adding using digital logic. Similarly a threshold element for a digital word would use a digital comparator. An accumulator for digital words would be a digital accumulator, not an analog one. In any of the circuits proposed by Vergnes et al., the handling of the digital words used to control the frequency of the phase would be done by using digital elements. Therefore, there would be no need for a gain element. The insertion of a gain stage in the Figure 6 embodiment of Vergnes et al. would have no function since the words being processed are digital. Thus, the specification teaches away from the modifications to Vergnes et al. proposed by the Examiner.

The Perrott reference is directed to a bit error rate detector. In a discussion of the prior art in Figure 1, Perrott does show a phase lock loop and does suggest a "loop amplifier." However, there is no series connection of an error filter, a gain element and a frequency accumulator. Perrott does not show a gain-accumulator combination.

With respect to the rationale for the combination of references, the Examiner states, on page 4 of the Office Action:

Vergnes et al. and Perrot [sic.] teachings teach in the same field of endeavor. Because loop amplifier and filter are implemented in the conventional PLL, one of ordinary skill in the art at the time the invention was made would have been motivated to modify Vergnes et al. PLL to further include a loop amplifier.

The Examiner's conclusion is incorrect. As noted above, Vergnes et al. has no need for a loop amplifier and therefore it would not be obvious to add one. The only motivation that exists for adding a loop amplifier to Vergnes et al. would be to meet

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the terms of the claim in a classical hindsight approach. The Examiner has demonstrated no reason for modifying Vergnes et al. by adding a loop amplifier. The Examiner has failed to establish a *prima facie* case of obviousness by establishing a rational for the combination of references.

As noted above, the purpose of the gain element in the specification is to provide control of overflow or underflow.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 01-0484 and please credit any excess fees to such deposit account.

Respectfully submitted,



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